11.3-Gbps Limiting Amplifier

FEATURES

- **Up to 11.3-Gbps Operation**
- **Loss-of-Signal Detection (LOS)**
- **Adjustable Output Voltage**
- **Low Power Consumption**
- **Input Offset Cancellation**
- **CML Data Outputs With On-Chip, 50-Ω Back-Termination to VCC**
- **Single 3.3 V Supply**
- **Surface-Mount, Small-Footprint, 3-mm × 3-mm, 16-Pin QFN Package**

APPLICATIONS

- **10 Gigabit Ethernet Optical Transmitters**
- **8× and 10× Fibre Channel Optical Transmitters**
- **SONET OC-192/SDH-64 Optical Transmitters**
- **XFP and SFP+ Transceiver Modules**
- **XENPAK, XPAK, X2 and 300-Pin MSA Transponder Modules**
- **Cable Driver and Receiver**

DESCRIPTION

The ONET1191P is a high-speed, 3.3-V limiting amplifier for copper-cable and fiber-optic applications with data rates up to 11.3 Gbps.

This device provides a gain of about 40 dB which ensures a fully differential output swing for input signals as low as 5 mV_{pp}. The output amplitude can be adjusted from 400 mV_{pp} to 700 mV_{pp}. Loss-of-signal detection and output disable are also provided.

The part is available in a small-footprint, 3-mm × 3-mm, 16-pin QFN package, typically dissipates less than 110 mW, and is characterized for operation from –40°C to 85°C.

BLOCK DIAGRAM

A simplified block diagram of the ONET1191P is shown in Figure 1.

This compact, low-power, 11.3-Gbps limiting amplifier consists of a high-speed data path with offset cancellation (dc feedback), a loss-of-signal detection block using two peak detectors, and a band-gap voltage reference and bias current generation block.

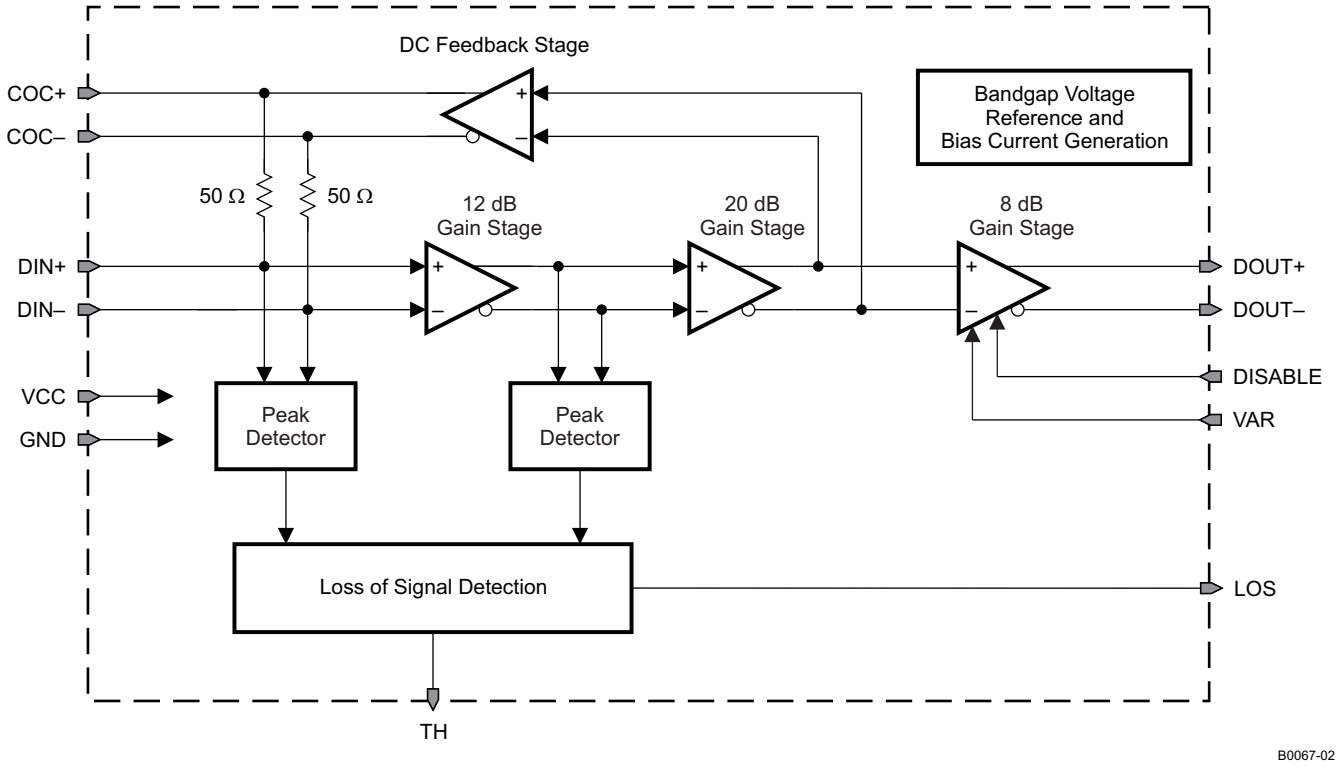


Figure 1. Simplified Block Diagram of the ONET1191P

HIGH-SPEED DATA PATH

The high-speed data signal is applied to the data path by means of the input signal pins, DIN+/DIN–. The data path consists of a 12-dB input gain stage with 2 × 50-Ω on-chip line-termination resistors, a second gain stage with 20 dB of gain, and a variable-gain output stage which provides another 8 dB of gain. The amplified data output signal is available at the output pins DOUT+/DOUT–, which include on-chip 2 × 50-Ω back-termination to VCC. The output amplitude can be adjusted between 400 mV_{pp} and 700 mV_{pp} by connecting an external resistor between the VAR pin and ground (GND).

A dc feedback stage compensates for internal offset voltages and thus ensures proper operation even for very small input data signals. This stage is driven by the output signal of the second gain stage. The signal is low-pass filtered, amplified, and fed back to the input of the first gain stage via the on-chip, 50-Ω termination resistors. The required low-frequency cutoff is determined by an external 0.1 µF capacitor, which must be differentially connected to the COC+/COC– pins.

LOSS-OF-SIGNAL DETECTION

The peak values of the input signal and output signal of the first gain stage are monitored by two peak detectors. The peak values are compared to a predefined loss-of-signal threshold voltage inside the loss-of-signal detection block. As a result of the comparison, the LOS signal, which indicates that the input signal amplitude is below the defined threshold level, is generated.

The threshold voltage can be set within a certain range by means of an external resistor connected between the TH pin and ground.

BAND-GAP VOLTAGE AND BIAS GENERATION

The ONET1191P limiting amplifier is supplied by a single 3.3-V supply voltage connected to the VCC pins. This voltage is referred to ground (GND).

On-chip band-gap voltage circuitry generates a reference voltage, independent of supply voltage, from which all other internally required voltages and bias currents are derived.

PACKAGE

For the ONET1191P, a small-footprint, 3-mm × 3-mm, 16-pin QFN package, with a lead pitch of 0,5 mm, is used. The pinout is shown in Figure 2.

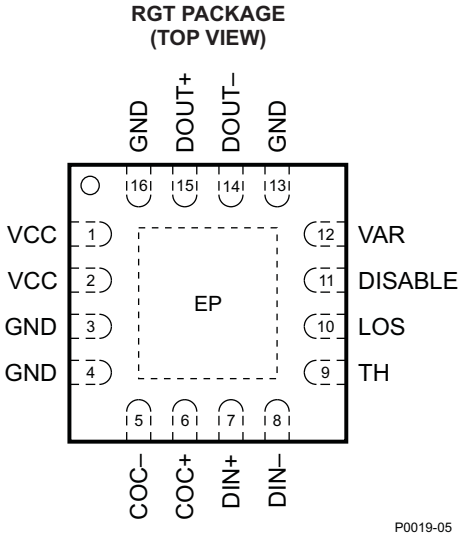


Figure 2. Pinout of ONET1191P in a 3-mm × 3-mm, 16-Pin QFN Package

TERMINAL FUNCTIONS

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
COC+	6	Analog	Offset cancellation filter capacitor plus terminal. An external 0.1 µF filter capacitor must be connected between this pin and COC– (pin 5).
COC–	5	Analog	Offset cancellation filter capacitor minus terminal. An external 0.1 µF filter capacitor must be connected between this pin and COC+ (pin 6).
DIN+	7	Analog input	Noninverted data input. On-chip, 50-Ω terminated to COC+. Differentially 100-Ω terminated to DIN–.
DIN–	8	Analog input	Inverted data input. On-chip, 50-Ω terminated to COC–. Differentially 100-Ω terminated to DIN+.
DISABLE	11	CMOS input	Disables the output stage when set to a high level
DOUT+	15	CML out	Noninverted data output. On-chip, 50-Ω back-terminated to VCC.
DOUT–	14	CML out	Inverted data output. On-chip, 50-Ω back-terminated to VCC.
GND	3, 4, 13, 16, EP	Supply	Circuit ground. Exposed die pad (EP) must be grounded.
LOS	10	Open-drain MOS	High level indicates that the input signal amplitude is below the programmed threshold level. Open-drain output. Requires an external 10-kΩ pullup resistor to VCC for proper operation.
TH	9	Analog input	LOS threshold adjustment with resistor to GND
VAR	12	Analog input	Variable output amplitude control. Output amplitude can be reduced to 400 mV_{pp} by grounding the VAR pin. Output amplitude can be set from 400 mV_{pp} to 700 mV_{pp} by connecting a 0 to 100-kΩ resistor to GND or leaving the pin open.
VCC	1, 2	Supply	3.3-V ±10% supply voltage

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE	UNIT
V_{CC}	Supply voltage(2)	–0.3 to 4	V
V_{DIN+}, $V_{DIN–}$	Voltage at DIN+, DIN–(2)	0.5 to 4	V
V_{LOS}, V_{COC+}, $V_{COC–}$, V_{TH}, V_{DOUT+}, $V_{DOUT–}$	Voltage at LOS, COC+, COC–, TH, DOUT+, DOUT–(2)	–0.3 to 4	V
$V_{DIN,DIFF}$	Differential voltage between DIN+ and DIN–	±1.25	V
I_{LOS}	Current into LOS	1	mA
I_{DIN+}, $I_{DIN–}$, I_{DOUT+}, $I_{DOUT–}$	Continuous current at inputs and outputs	20	mA
ESD	ESD rating at all pins	1.5	kV (HBM)
$T_{J,max}$	Maximum junction temperature	125	°C
T_{STG}	Storage temperature range	–65 to 85	°C
T_A	Characterized free-air operating temperature range	–40 to 85	°C
T_{LEAD}	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	2.9	3.3	3.6	V
T_A	Operating free-air temperature	–40		85	°C
	Disable input high voltage	2			V
	Disable input low voltage			0.25	V
	Optimum LOS threshold resistor	32		62	kΩ
	R_{VAR} range	0		open	kΩ

DC ELECTRICAL CHARACTERISTICS

over recommended operating conditions, outputs connected to a 50-Ω load, R_{VAR} = open (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		2.9	3.3	3.6	V
I_{VCC}	Supply current	DISABLE = LOW		33	49	mA
R_{IN}	Data input resistance	Single-ended to COC pins		50		Ω
R_{OUT}	Data output resistance	Single-ended, referenced to V_{CC}		50		Ω
	Voltage at TH pin			1.25		V
	LOS HIGH voltage	10-kΩ pullup to V_{CC}, I_{SOURCE} = 50 µA	2.4			
	LOS LOW voltage	10-kΩ pullup to V_{CC}, I_{SINK} = 200 µA			0.5	V

AC ELECTRICAL CHARACTERISTICS

over recommended operating conditions, outputs connected to a 50-Ω load, R_{VAR} = open (unless otherwise noted). Typical operating condition is at V_{CC} = 3.3 V and T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{3dB-H}	High-frequency –3-dB bandwidth		8	11	15	GHz
f_{3dB-L}	Low-frequency –3-dB bandwidth	C_{OC} = 0.1 µF, ac coupling capacitors = 0.1 µF		30		kHz
$v_{IN,MIN}$	Data input sensitivity	K28.5 at 11.3 Gbps, BER < 10^{-12}		2.5	5	mV_{pp}
		$V_{OD-min} \geq 0.95 \times V_{OD}$ (output limited)		10	20	
A	Small-signal gain		34	40	44	dB
$V_{IN,MAX}$	Data input overload		2000			mV_{pp}
DJ	Deterministic jitter	V_{IN} = 5 mV_{pp}, K28.5 at 11.3 Gbps		4	7	ps_{pp}
		V_{IN} = 20 mV_{pp}, K28.5 at 11.3 Gbps		4	9	
RJ	Random jitter	Input = 5 mV_{pp}		1.6		ps_{RMS}
		Input = 20 mV_{pp}		0.7		
V_{OD}	Differential data output voltage	$V_{IN} \geq$ 20 mV_{pp}, DISABLE = LOW	600	700	900	mV_{pp}
		DISABLE = HIGH		25	100	
t_r	Output rise time	20% to 80%, $V_{IN} \geq$ 20 mV_{PP}		25	35	ps
t_f	Output fall time	20% to 80%, $V_{IN} \geq$ 20 mV_{PP}		25	35	ps
V_{TH}	LOS assert threshold range	K28.5 pattern at 10.7 Gbps, R_{TH} = 62 kΩ		40		mV_{pp}
		K28.5 pattern at 10.7 Gbps, R_{TH} = 32 kΩ		65		
	LOS threshold variation	Versus temperature		3		dB
		Versus supply voltage V_{CC}		1		dB
	LOS hysteresis	K28.5 pattern at 11.3 Gbps	1.5		7	dB
t_{LOS_AST}	LOS assert time			1300	2000	ns
$t_{LOS,\ DEA\_}$	LOS deassert time			120		ns
t_{DIS}	Disable response time			90		ns

TYPICAL OPERATION CHARACTERISTICS

Typical operating condition is at V_{CC} = 3.3 V, T_A = 25°C, and R_{VAR} = open (unless otherwise noted)

FREQUENCY RESPONSE

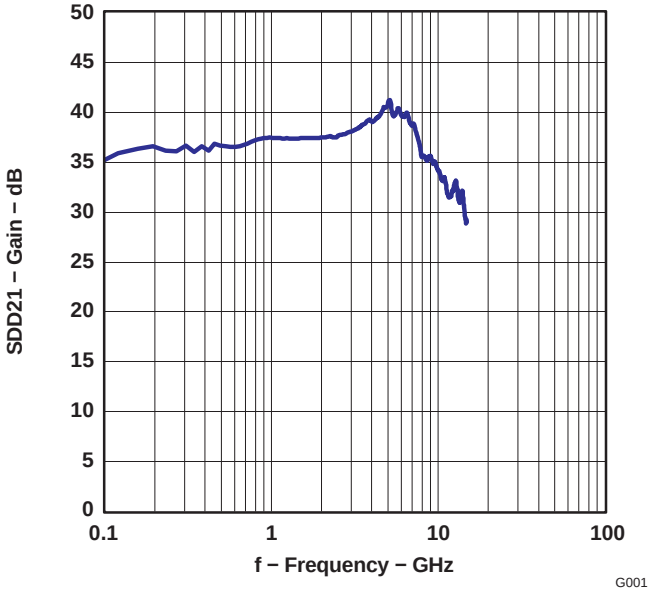


Figure 3.

TRANSFER FUNCTION

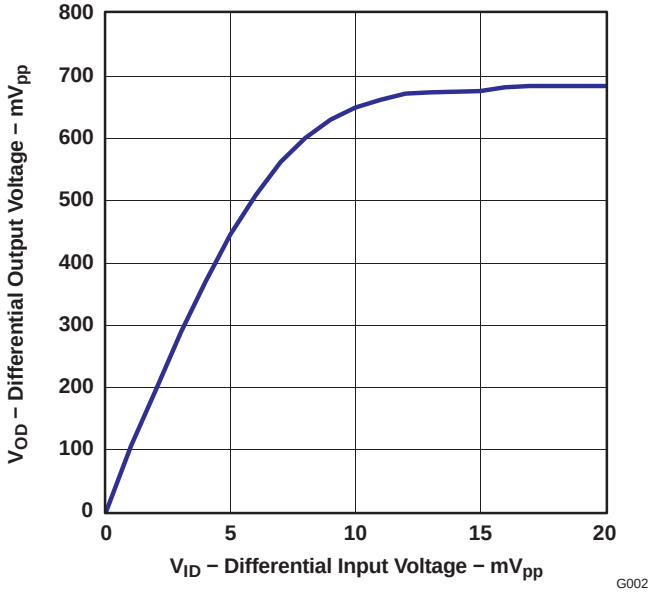


Figure 4.

DIFFERENTIAL INPUT RETURN GAIN
vs
FREQUENCY

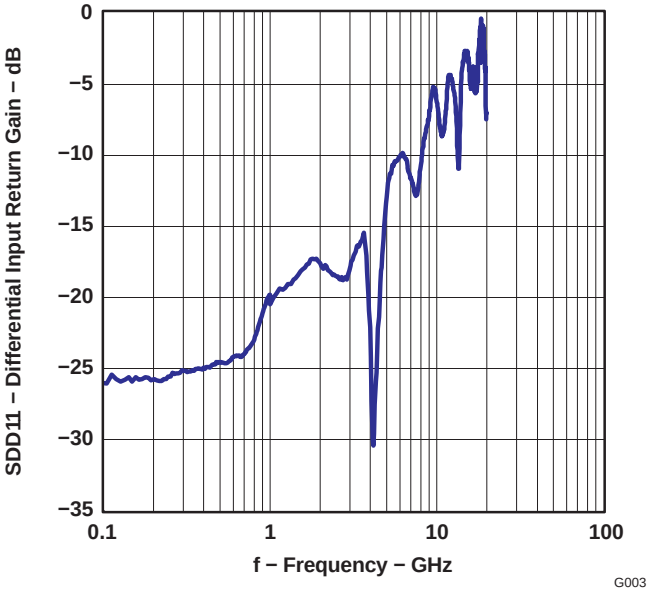


Figure 5.

DIFFERENTIAL OUTPUT RETURN GAIN
vs
FREQUENCY

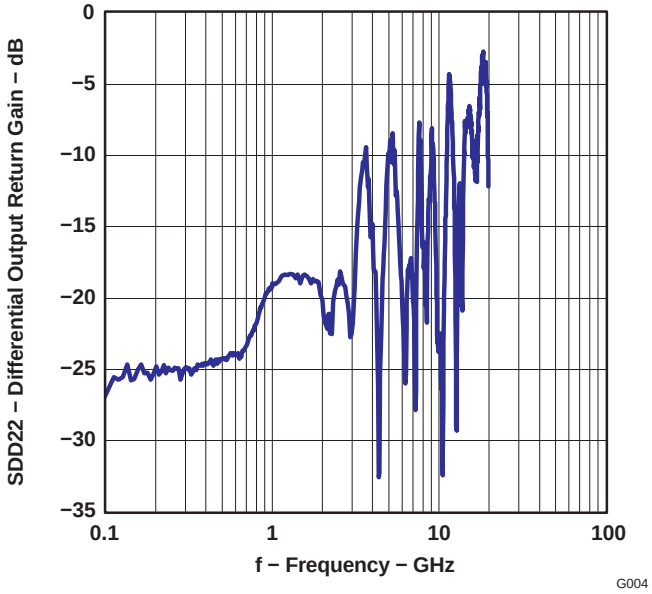


Figure 6.

TYPICAL OPERATION CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3 V, T_A = 25°C, and R_{VAR} = open (unless otherwise noted)

BIT-ERROR RATIO vs INPUT AMPLITUDE (11.3 GBPS)

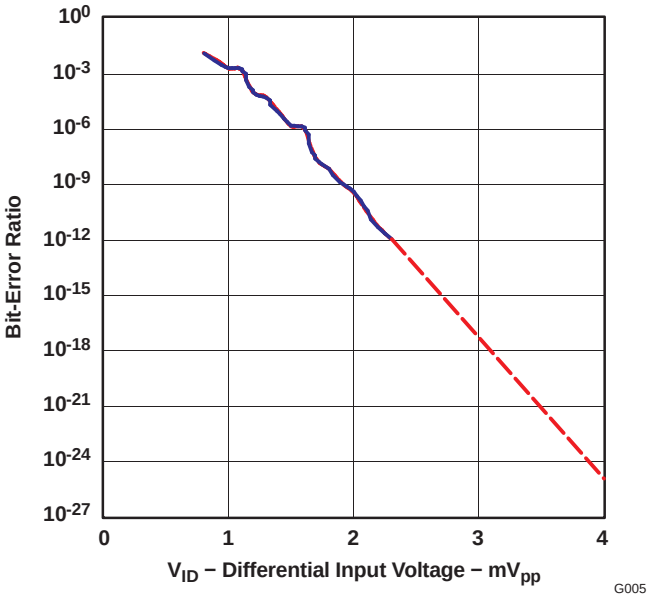


Figure 7.

DETERMINISTIC JITTER vs INPUT AMPLITUDE

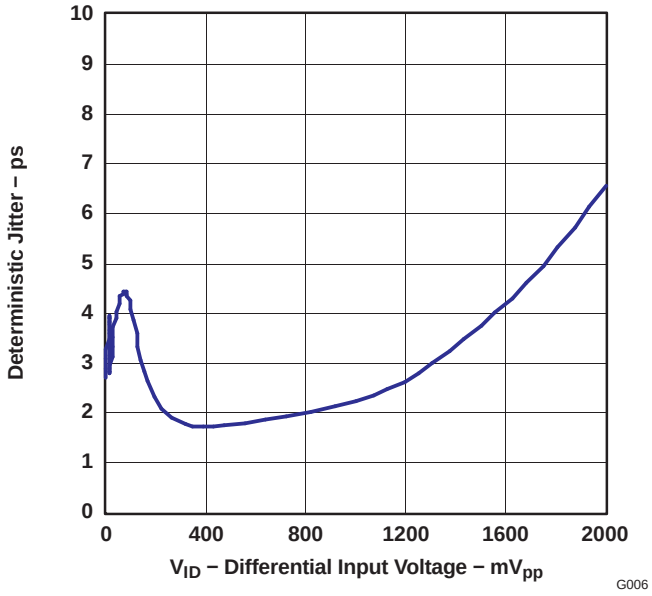


Figure 8.

RANDOM JITTER vs INPUT AMPLITUDE

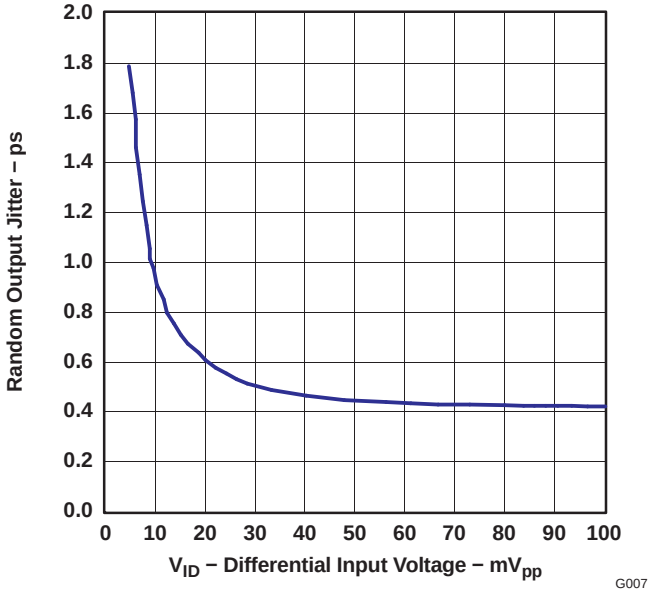


Figure 9.

LOS ASSERT/DEASSERT VOLTAGE vs THRESHOLD RESISTANCE

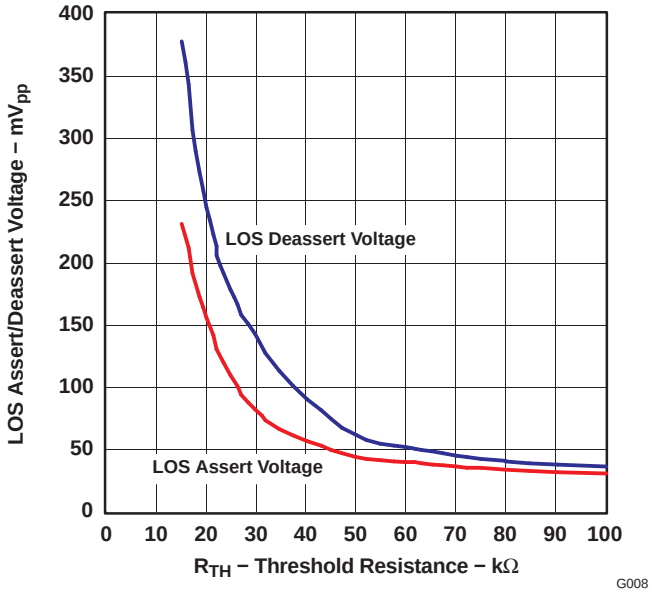


Figure 10.

TYPICAL OPERATION CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3 V, T_A = 25°C, and R_{VAR} = open (unless otherwise noted)

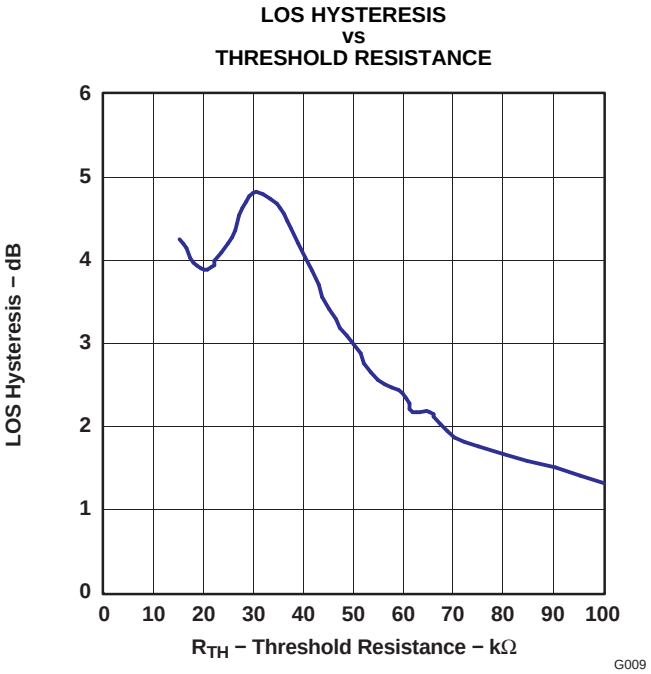


Figure 11.

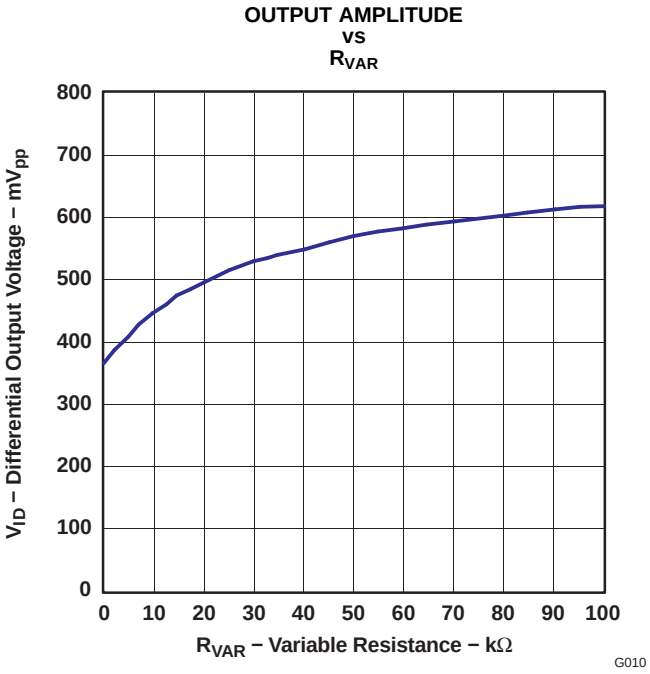


Figure 12.

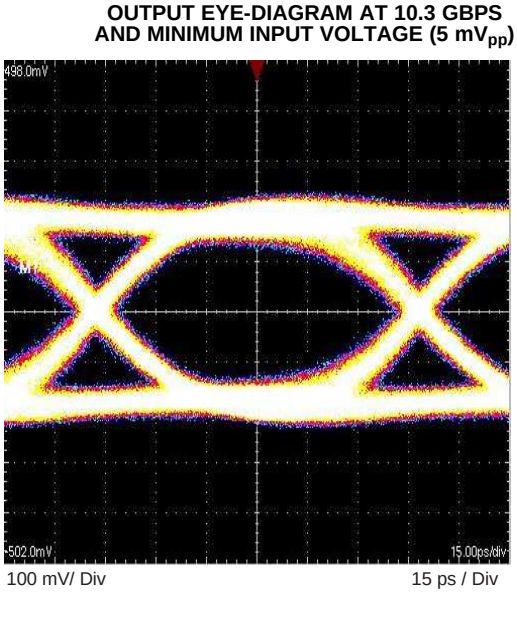


Figure 13.

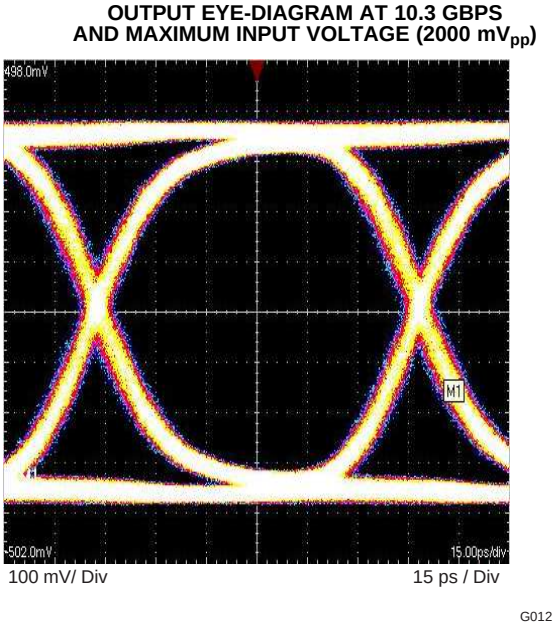


Figure 14.

TYPICAL OPERATION CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3 V, T_A = 25°C, and R_{VAR} = open (unless otherwise noted)

OUTPUT EYE-DIAGRAM AT 8.5 GBPS AND MINIMUM INPUT VOLTAGE (5 mV_{pp})

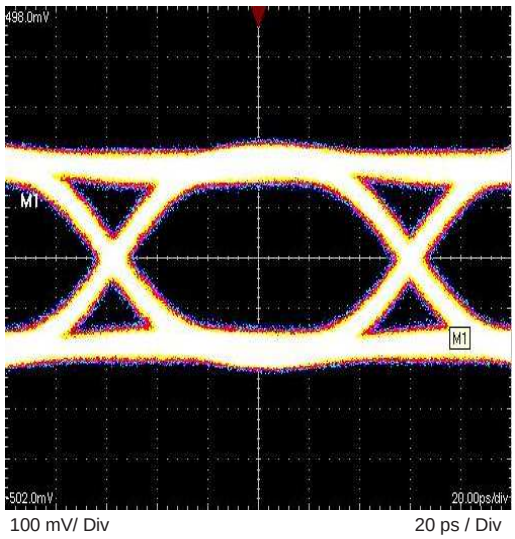


Figure 15.

OUTPUT EYE-DIAGRAM AT 8.5 GBPS AND MAXIMUM INPUT VOLTAGE (2000 mV_{pp})

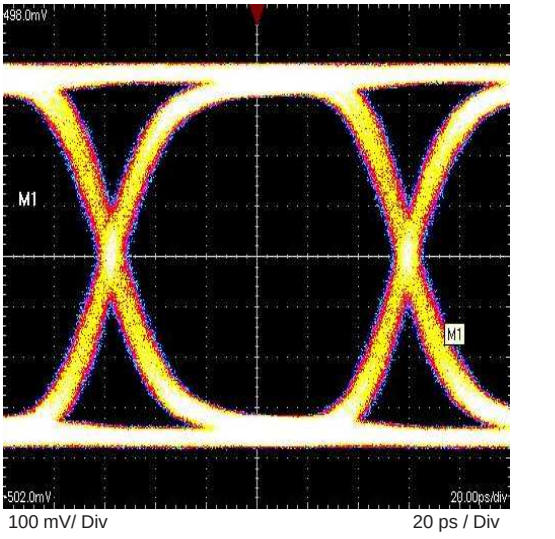


Figure 16.

APPLICATION INFORMATION

Figure 17 shows a typical application circuit using the ONET1191P. The output amplitude can be adjusted with R_{VAR} and the LOS assert voltage is adjusted with R_{TH}.

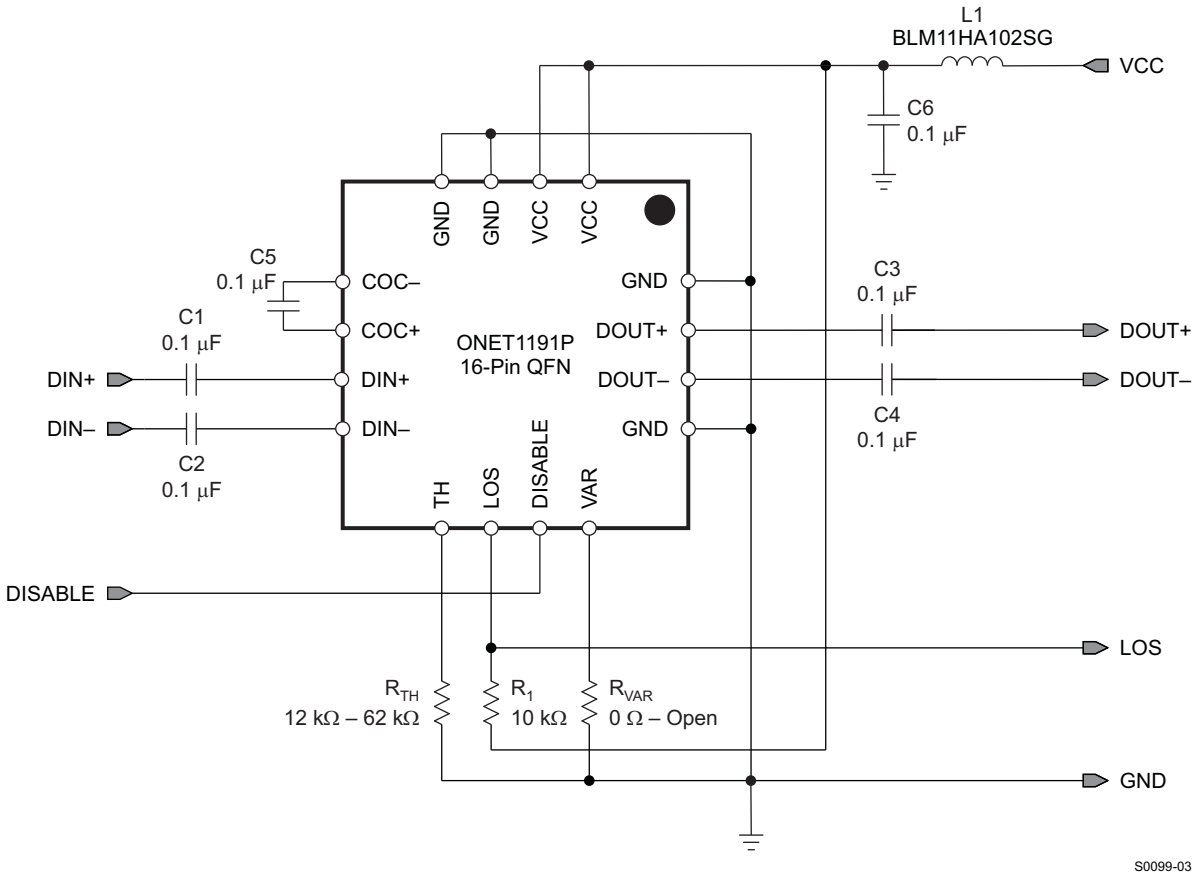


Figure 17. Basic Application Circuit

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
ONET1191PRGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ONET1191PRGTRG4	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ONET1191PRGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ONET1191PRGTTG4	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

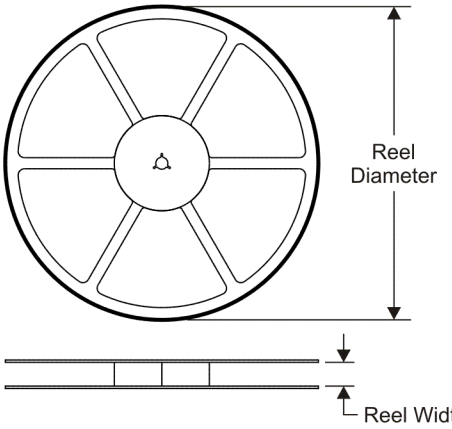
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

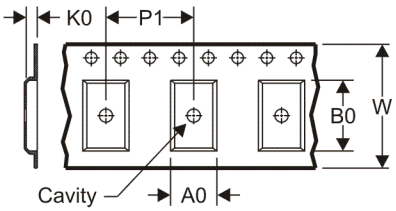
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

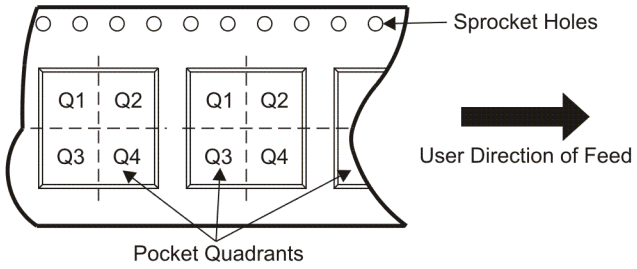


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

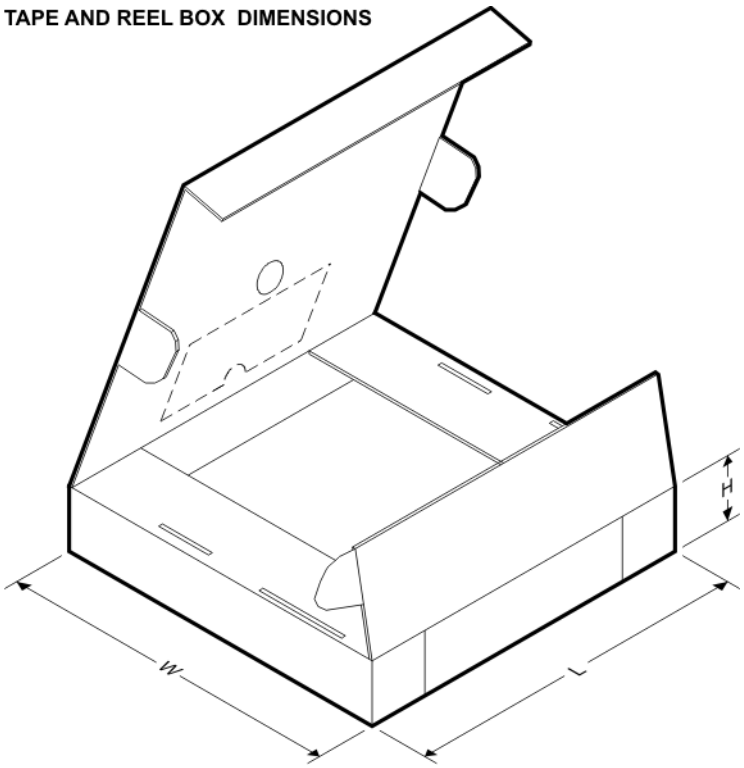
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ONET1191PRGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ONET1191PRGTT	QFN	RGT	16	250	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

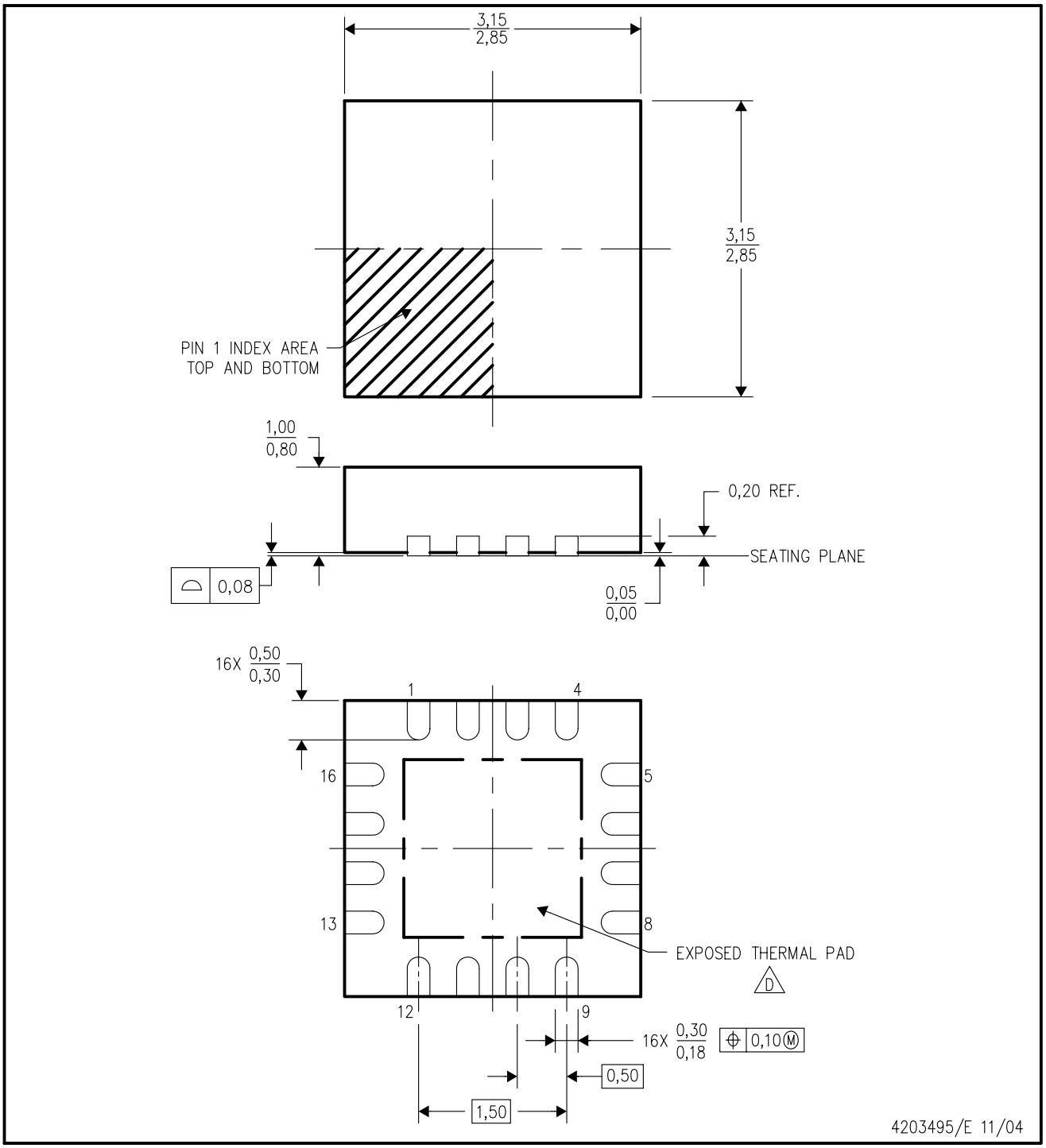
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ONET1191PRGTR	QFN	RGT	16	3000	340.5	333.0	20.6
ONET1191PRGTT	QFN	RGT	16	250	340.5	333.0	20.6

RGT (S–PQFP–N16) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

THERMAL PAD MECHANICAL DATA

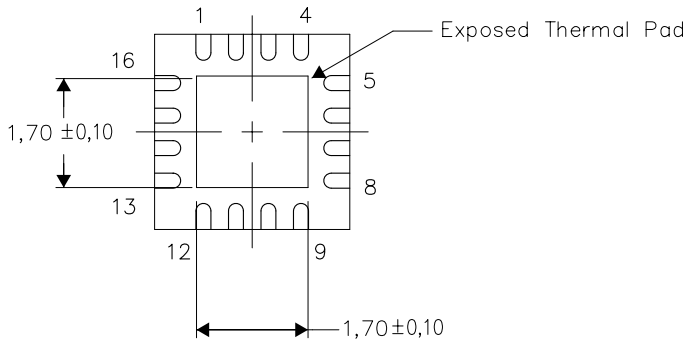
RGT (S–PQFP–N16)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

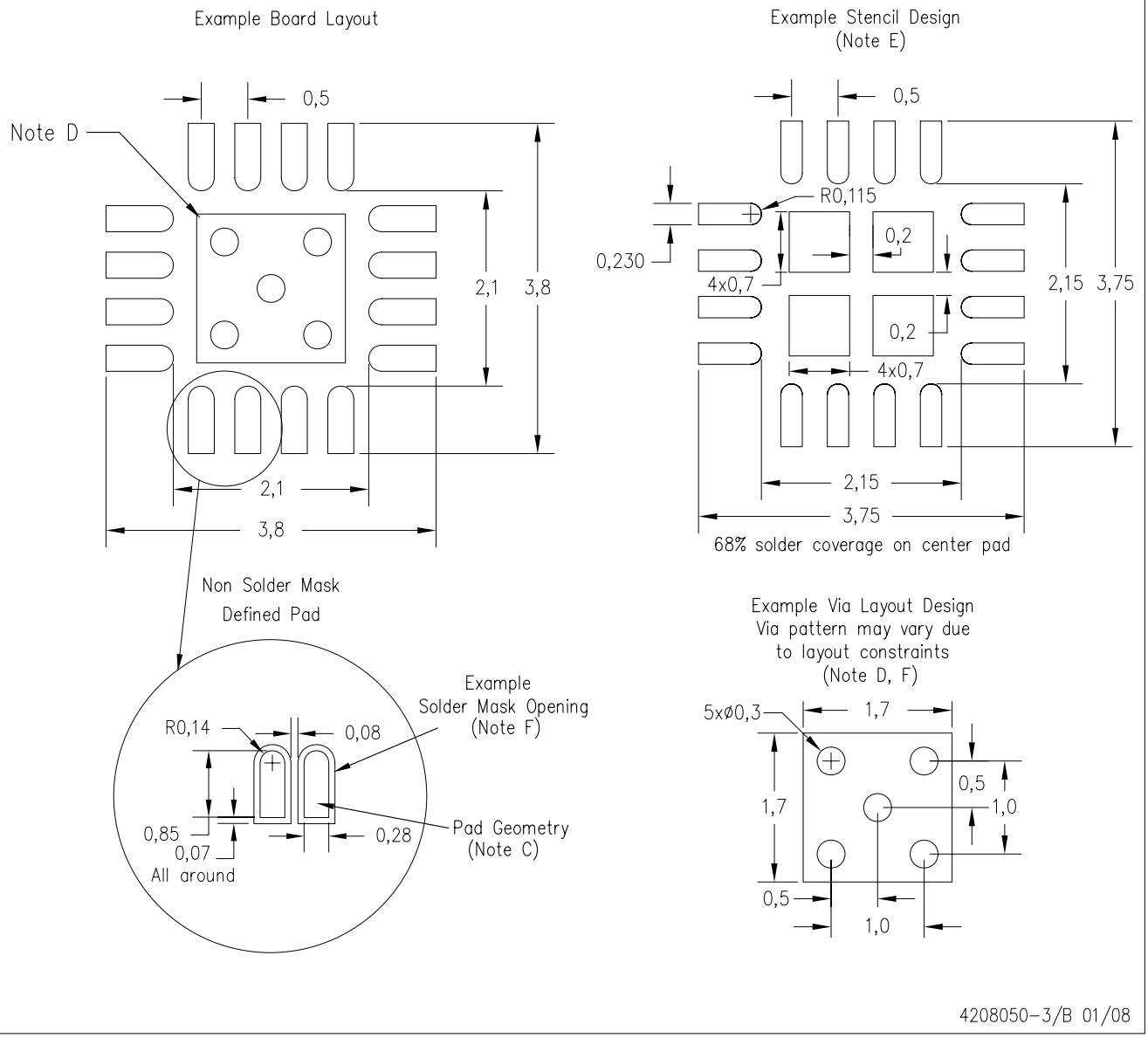


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGT (S–PQFP–N16)



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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